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(54) Measuring the frequency of a sinusoidal signal

(57) A device for the high-resolution measurement of the rotational speed of a shaft by means of a signal generator 1, which generates a sinusoidal signal 1.3, includes a signal processing unit 3 in which the sinusoidal signal is digitized at 3.1 and examined for zero transitions with a falling edge and is correspondingly evaluated. A flip-flop 4.1 produces an output pulse at each such transition which triggers an adder ADD 1 to add the absolute amplitudes of the sinusoidal signal at sample points immediately preceding and following the transition. The adder output is divided at DIV 1 by the absolute amplitude immediately following the transition, and the output of DIV 1 is added, ADD 2, to the output of a counter Z counting the number of sampling pulses occurring between successive pulses from the flip-flop 4.1. The output of DIV 1 in the previous cycle, held in a memory DSP 2, is then subtracted, SUB, from the output of ADD 2, and the resulting signal multipled, MULT 1, by a signal derived from the sampling period and the number of teeth used in signal generator 1. The result in seconds per revolution of transmitter 1. 1 may be translated into revolutions per minute in divider DIV 2.

Fig.1

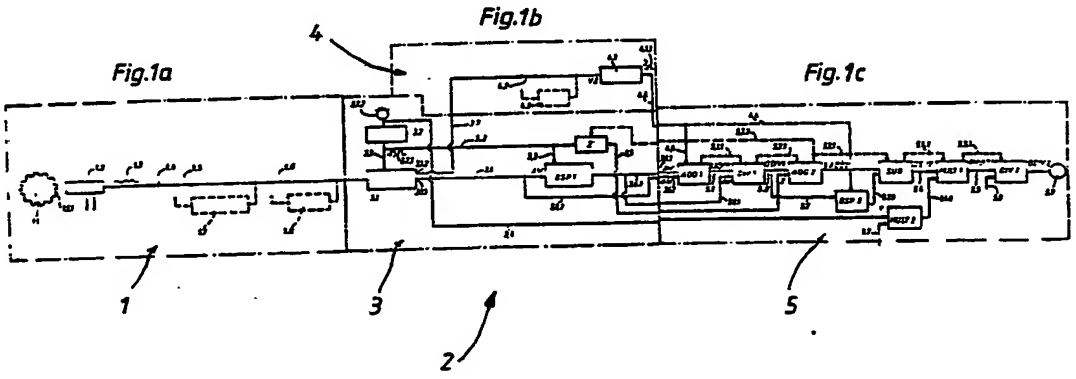

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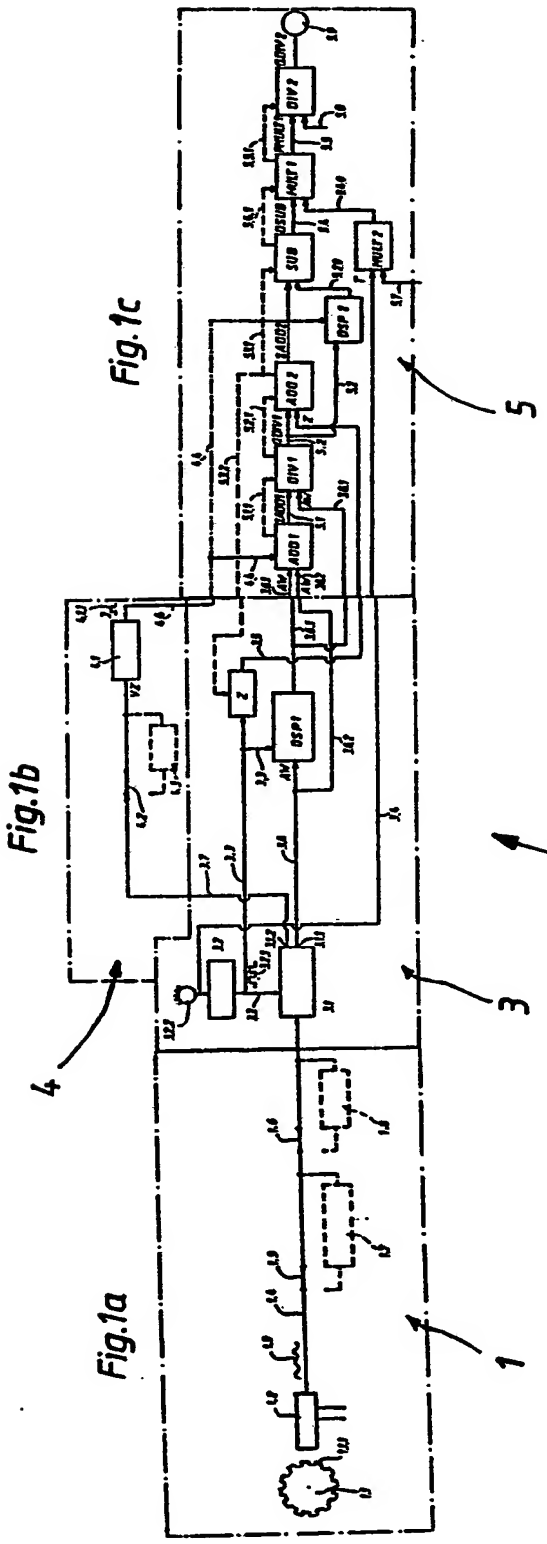
Fig.1



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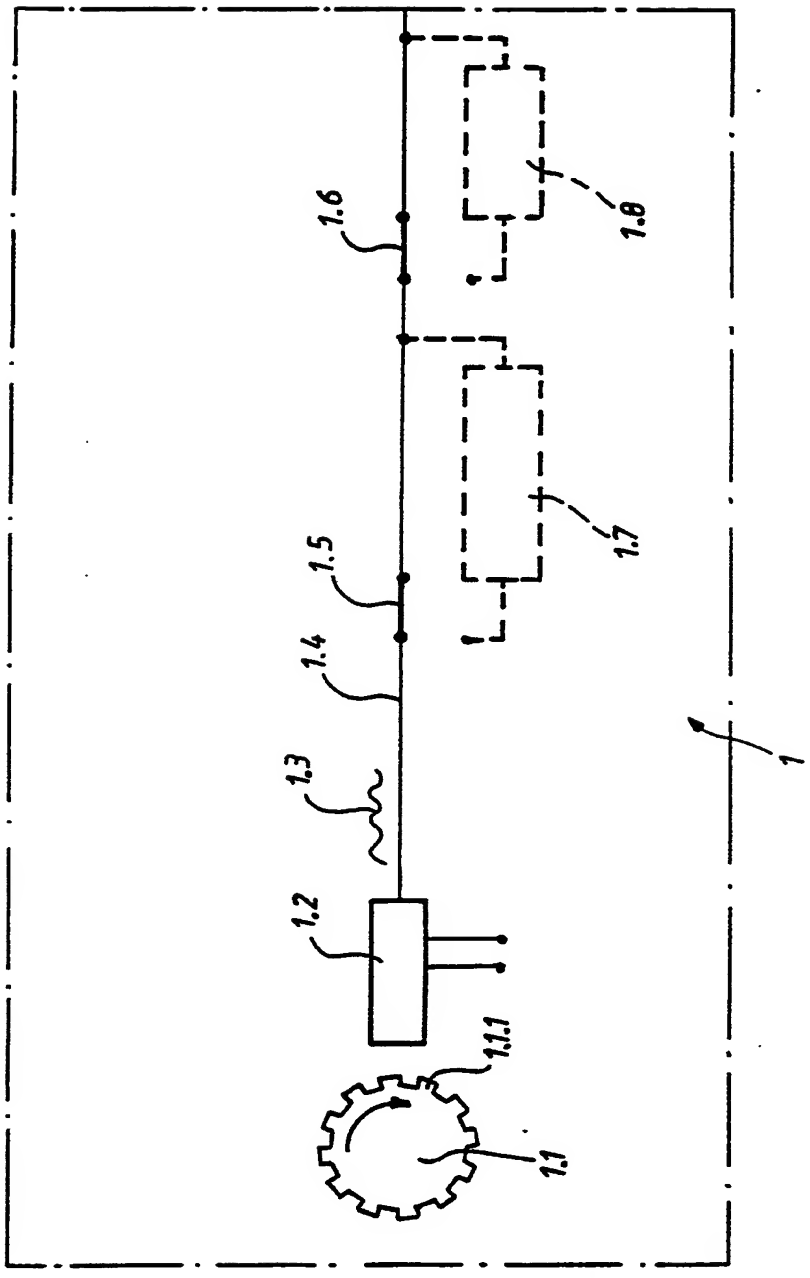

Fig.1a

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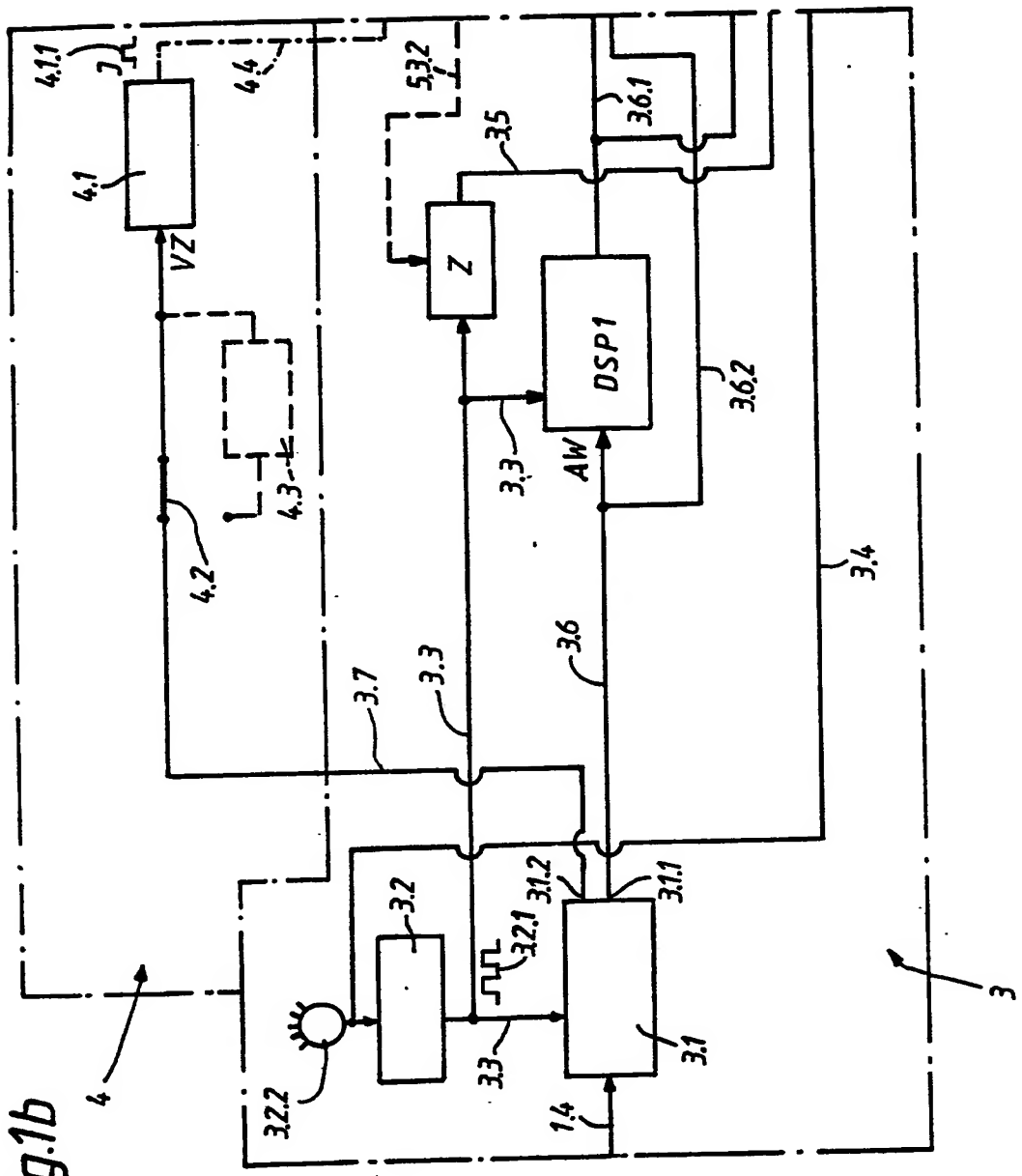

Fig.1b

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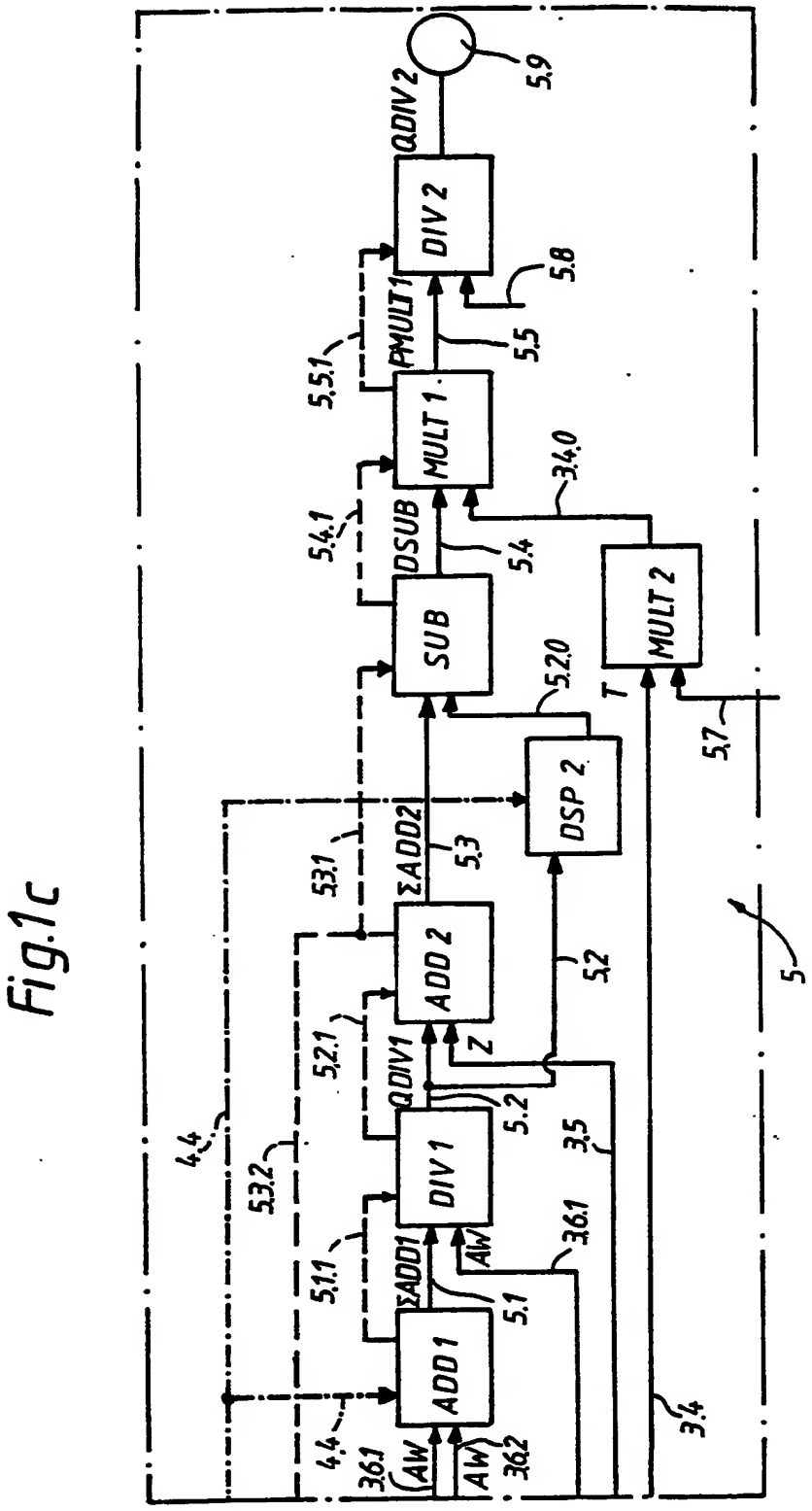

Fig.1c

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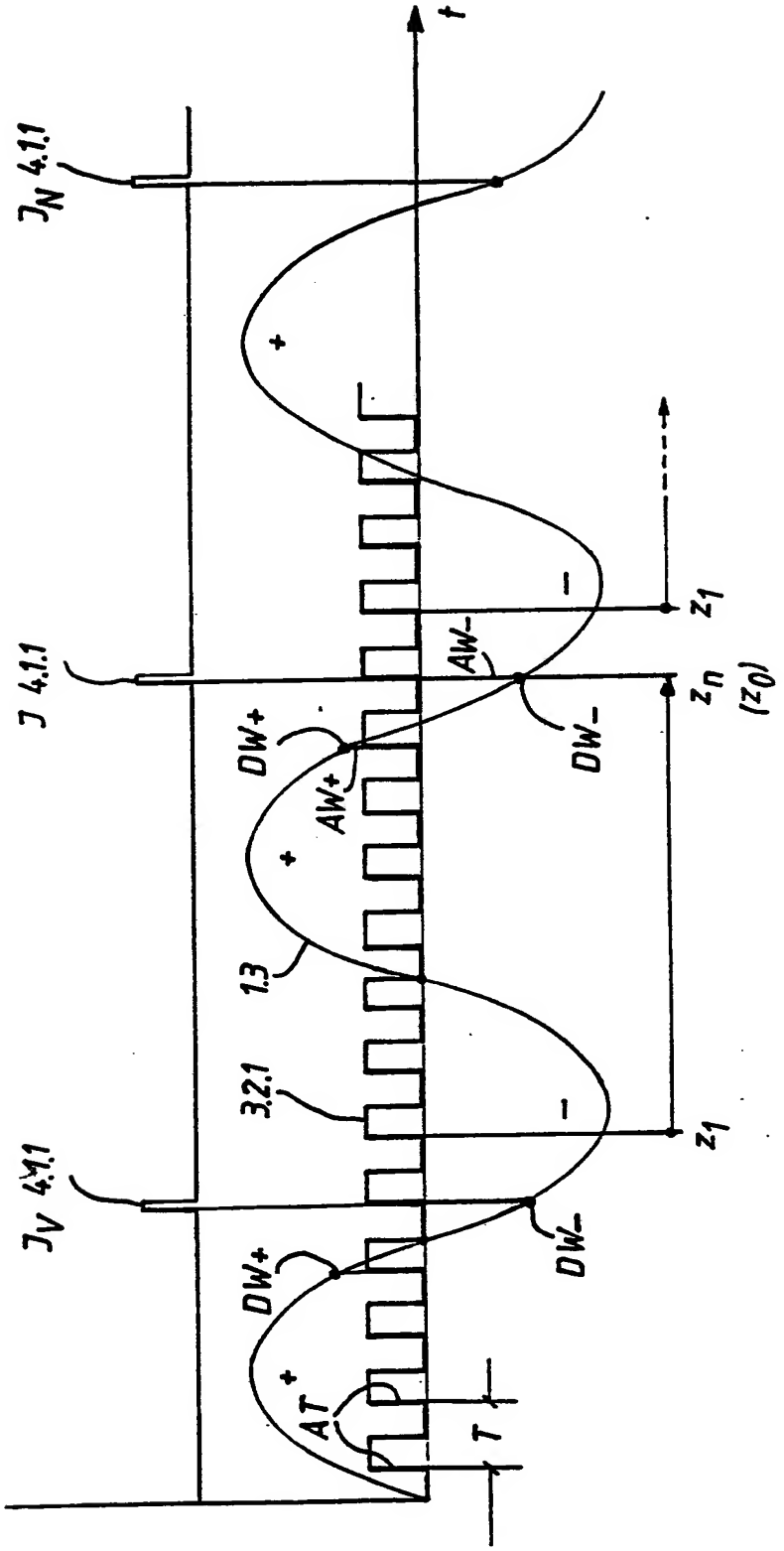

Fig.2

A device for measuring the frequency of a sinusoidal signal generated by a signal generator

The invention relates to a device for measuring the frequency of a sinusoidal signal generated by a signal generator for measuring the rotational speed of a shaft by means of the signal generated by a signal generator comprising a transmitter which revolves with the shaft and has uniform divisions and a sensor, which device includes a signal processing unit containing an oscillator, A/D converter, counter and memory, the sinusoidal signal being supplied, in operation, to the A/D converter of the signal processing unit.

Devices are generally known in which either the periods of the sinusoidal signal generated are counted out within a particular gate time or clock pulses are counted out during the periods of the signal generated and are correspondingly evaluated in a signal processing unit for obtaining information on the frequency rotational speed (for example German Patent Specification No. 31 25 197).

In addition, a device is known (US Patent Specification No. 4 363 099) by means of which the frequency of a sinusoidal signal, but in particular a deviation from the known and largely constant frequency can be determined without requiring a zero transition determination. In this arrangement, a large number of measurements is performed per period of the sinusoidal signal for forming digital values which are stored and from which the frequency is then determined by linear interpolation and formula relations.

The present invention seeks to develop a generic device in such a manner that a high-resolution determination is also possible of an unknown frequency or rotational speed of a shaft with the least measurement expenditure.

According to the invention, there is provided a device for measuring the frequency of a sinusoidal signal generated by a signal generator for measuring the

rotational speed of a shaft by means of the signal generated by a signal generator comprising a transmitter which revolves with the shaft and has uniform divisions and a sensor, which device includes a signal processing unit containing an oscillator, A/D converter, counter and memory, the sinusoidal signal being supplied, in operation, to the A/D converter of the signal processing unit, which converter is activated by the oscillator with a constant but adjustable sampling clock frequency - which is higher than the signal frequency - and which in each case forms from the sinusoidal signal digital values which are associated with the sampling clock pulses,wherein

- the A/D converter applies the digital values DW to its outputs in accordance with sign VZ and absolute value AW, the sign VZ being supplied to a flip-flop stage,

- and, triggered by each sampling clock pulse AT of the oscillator via a clock line, on the one hand both a first digital memory (DSP 1) is activated which then accepts the absolute value AW of the digital value formed during the preceding clock pulse which happens to be present at the output of the A/D converter, and supplies this value both to an adder (ADD 1) and to a divider (DIV 1), and the counter (Z) is incremented by "1", the incremented count being supplied to an adder (ADD 2), on the other hand the A/D converter is activated, and now forms the next digital value and applies the latter to its outputs in accordance with sign VZ and absolute value AW, this next absolute value AW also being supplied to the adder (ADD 1),

- and an output pulse is only generated by the flip-flop stage when the sign VZ changes from positive to negative or vice-versa, which output pulse activates both the adder (ADD 1) and a second digital memory (DSP 2) via a pulse line, whereupon the adder (ADD 1) adds the absolute value (AW +) of the last positive digital value, supplied by the digital memory (DSP 1), to the absolute value (AW -) of the first negative digital value and, after completion of the arithmetic operation, activates

the divider (DIV 1), which forms the quotient of the absolute value (AW +) of the last positive digital value and the result $\leq$ ADD 1 of the adder (ADD 1), and, after completion of the arithmetic operation, activates the adder (ADD 2), which adds the result Q DIV 1 of the divider (DIV 1) to the count Zn reached between the preceding (J_v) and the present output pulse (J), when the first negative digital value is present, and, after completion of the arithmetic operation, on the one hand resets the counter (Z) to "0" and on the other hand activates a subtracting unit (SUB) which forms the difference of the result $\leq$ ADD 2 of the adder (ADD 2) and the content Q DIV1$_v$ of the digital memory (DSP 2),
the result Q DIV 1$_v$ having been obtained in the arithmetic operations triggered by the preceding output pulse (J_v) and transferred into the digital memory (DSP 2) during the present output pulse (J), whilst the present result QDIV 1 is only transferred into the digital memory (DSP 2) during the subsequent output pulse (J_N),
and, after completion of the arithmetic operation, activates a multiplier (MULT 1) which forms the product of the result SDSUB of the subtracting unit (SUB) and a signal-generator-specific product present via the input,

- and the frequency or rotational speed is measured again by the output pulse (J_N) generated during the next zero transition of the sinusoidal signal from positive to negative or vice-versa.

Preferably, the scanning clock frequency is a multiple of the signal frequency of the sinusoidal signal, in which case,
at high rotational speed and in consequence high signal frequency, a high sampling clock frequency is set. The digital values of the A/D converter are preferably output in binary complement code.

The flip-flop stage may comprise an edge-controlled, monostable flip-flop and an inverter may be connected in series with the flip-flop stage via a change-over switch. An amplifying and/or offset section may be connected

between the sensor and the A/D converter, and a low-pass filter may be connected between the sensor and the A/D converter.

The signal-generator-specific product may be manually input as an amount to the multiplier (MULT 1) via the input.

The signal-generator-specific product may be supplied to the multiplier (MULT 1) from a multiplier (MULT 2) at the inputs of which the sampling period T of the sampling clock frequency is present via a line and the number of the transmitter divisions via an input line. The multiplier (MULT 1), after completion of its arithmetic operation, may activate a divider (DIV 2) which forms the quotient Q DIV 2 (revolution per minute) from the number "60" and the result PMULT 1 (seconds per revolution).

Thus conclusions, for example with respect to the condition of an internal combustion engine, can be drawn from the high-resolution rotational speed information by means of suitable analysis in that, for example, information on the torque can be obtained from the changes in rotational speed during one or more operating cycles-even in non-steady-state operation. By combining these information items with other signals sampled at the same time, conclusions can be drawn with respect to error sources, for example in the workshop area or in production control. Since, in addition, analogous measurement values are registered during the other measurement value recordings taken on the engine and on the vehicle, this device can be advantageously integrated into the existing recording systems.

An embodiment of the invention will now be described in greater detail in the text which follows by way of example with reference to the drawing, in which:

Figure 1 shows a block diagram of a device according to the invention, and

Figure 2 shows a timing chart of the signals and pulses.

The device essentially comprises four units; a

signal generator unit 1 and a signal processing unit 2 consisting of a signal sampling unit 3, a comparator unit 4 and an evaluating unit 5.

The signal generator unit 1 comprises a transmitter 1.1 which is connected to a shaft - the rotational speed of which must be measured - which is provided with uniform divisions 1.1.1 and which are formed as teeth or light/dark markings. The transmitter 1.1 itself can be formed, for example, by the starter gear ring on the fly wheel of an engine. A sensor (1.1), which is constructed as inductive, capacitive or optical sensor, is arranged adjacently to the divisions 1.1.1 of the transmitter 1.1. The sinusoidal signal 1.3 generated by the sensor when the transmitter is rotating is supplied via a line 1.4 to an A/D converter 3.1 of the signal sampling unit 3, in which arrangement an amplifying and/or offset section 1.7 and a low-pass filter 1.8 can be looped into the line 1.4 via switches 1.5 and 1.6. Whilst the amplifying and/or offset section 1.7 has the effect of optimally matching the sinusoidal signal to the acceptance range of the A/D converter 3.1, the low-pass filter 1.8 eliminates high frequency interference in the sinusoidal signal whilst the useful frequency can pass unimpeded.

In addition to the A/D converter 3.1, the signal sampling unit 3 contains an oscillator 3.2 for generating a sampling clock frequency 3.2.1 - the sampling period of which can be set via a corresponding adjusting section 3.2.2 - and a counter Z and a digital memory DSP 1. The oscillator 3.2 is connected to the A/D converter 3.1, the counter Z and the digital memory DSP 1 via a clock line 3.3. Via a line 3.4, the sampling period T (sec) set at the adjusting section 3.2.2 is transferred to a multiplier MULT 2 and, via a line 3.5, the respective count Z_x is transferred to an adder ADD 2 of the evaluation unit 5. One output 3.1.1. of the A/D converter 3.1 is connected via a line 3.6 to the digital memory DSP 1 to which, via a line 3.6.1, both an adder ADD 1 and a divider DIV 1 of the evaluating unit 5 are connected, the adder ADD1

furthermore also being connected via a line 3.6.2. to the output 3.1.1 of the A/D converter 3.1. The other output 3.1.2 of the A/D converter 3.1 is connected via a sign line 3.7 to an edge-controlled monostable flip-flop stage 4.1 - for example TTL 74 121 - of the comparator unit 4, in which arrangement an inverter 4.3 can be looped into the sign line 3.7 via a change over switch 4.2.

Within the evaluating unit 5, the adder ADD 1 is connected both via a signal line 5.1 and via a command line 5.1.1 to the divider DIV 1, which is connected via a signal line 5.2 and command line 5.2.1 to the adder ADD 2, which is connected via signal line 5.3 and a command line 5.3.1. to a subtracting unit SUB which is connected via signal line 5.4 and a command line 5.4.1 to a multiplier MULT 1 which, in turn, is connected via a signal line 5.5 and a command line 5.5.1 to a divider DIV 2. Furthermore, another digital memory DSP 2 which, in turn, is also connected to the subtracting unit SUB via signal line 5.2.0, is connected to the divider DIV 1 via the signal line 5.2. Similarly, the adder ADD 2 is also connected to the counter Z via a command line 5.3.2 and the multiplier MULT 2 is also connected to the multiplier MULT 1 via a signal line 3.4.0. Values are still input both to the multiplier MULT 2 and to the divider DIV 2 via input lines 5.7 and 5.8, thus, the "number of transmitter divisions 1.1.1" to the multiplier via the input line 5.7 and the dividend "60" to the divider via the input line 5.8.

Furthermore, the flip-flop stage 4.1 is connected via a pulse line 4.4 both to the adder ADD 1 and to the digital memory DSP 2 for transmitting an output pulse 4.1.1 generated by it.

The device operates as follows and is explained in greater detail with reference to Figures 1 and 2;

Due to the transmitter 1 with its divisions 1.1.1, which rotates with the shaft, a sinuosidal signal 1.3 is generated in the sensor 1.2 which is supplied to the A/D converter 3.1. The A/D converter 3.1 is activated by the oscillator 3.2 via the clock line 3.3 with a constant

sampling clock frequency 3.2.1. which is a multiple - at least twice - the signal frequency of the signal 1.3 and is correspondingly predetermined at the adjusting section 3.2.2 in dependence on the rotational speed of the shaft. With each sampling clock pulse, the A/D converter 3.1 forms the sinusoidal signal a digital value DW associated with the sampling clock pulse and applies this value to output 3.1.1 in accordance with its absolute value AW and to output 3.1.2 in accordance with its sign VZ. The sinusoidal analog signal 1.3 is thus correspondingly digitized, the digital value being represented as conversion result, for example in binary complement code (where the value "+1" is output as 0001, the value " - 1" as 1111, the value " + 2" as 0010, the value "-2" as 1110 and so forth, the first digit containing the sign).

Let it be assumed, then, that the last positive digital value DW +, and thus its absolute value AW + and its sign VZ +, have been formed in the A/D converter 3.1 by a sampling clock pulse from the positive half wave of the sinusoidal signal and have been applied to the outputs 3.1.1 and 3.1.2 so that the sign VZ + is also present, via the sign line 3.7 and the change-over switch 4.2, which is closed in this line, at flip-flop stage 4.1 and the absolute value AW + is also present both at the digital memory DSP 1 via line 3.6 and at the adder ADD 1 via line 3.6.2. line 3.6 and at the adder ADD 1 via line 3.6.2.

During the next sampling clock pulse, on the one hand the digital memory DSP 1 is activated via the clock line 3.3, which memory then accepts the absolute value AW + present at it, and on the other hand the count of the counter Z is incremented by "1".

Furthermore, the A/D converter 3.1 is activated via the clock line 3.3, which converter then forms the first negative digital value DW-, and thus its absolute value AW - and its sign VZ -, from the first negative half wave of the sinusoidal signal. The negative sign VZ - then present at the output 3.1.2 is also applied, via the sign line 3.7, to the flip-flop stage 4.1 whereupon the latter

switches due to the change of sign from "+" to "-" and generates an output J 4.1.1 which activates both the adder ADD 1 and the digital memory DSP 2 via the pulse line 4.4. The absolute value AW - present at the output 3.1.1 is applied both to the digital memory DSP 1 via line 3.6 and to the adder ADD 1 via line 3.6.2. As the adder ADD 1 is activated by the output pulse J 4.1.1, the adder ADD 1 accepts both the stored absolute value AW + from the digital memory DSP 1 and the absolute value AW present via the line 3.6.2 and adds then together. After completion of the arithmetic operation, it activates, via command line 5.1., the divider DIV 1 which then accepts the result ΣADD 1 of the adder ADD 1, which is present via the signal line 5.1, and the - stored - absolute value AW +, which is present via the line 3.6.1, and forms the quotient of the absolute value AW + and the result Σ ADD 1. After completion of the arithmetic operation, it activates, via the command line 5.2.1, the adder ADD 2 which then takes over the result QDIV 1 of the divider DIV 1, present via the signal line 5.2, and the count Zn of the counter Z, present via the line 3.5, and adds these two values.

In this context, the count Zn corresponds to the number of sampling clock pulses which were generated between the preceding output pulse Jv and the present output pulse J. After completion of the arithmetic operation, on the one hand the count of the counter Z is reset back to "0" by the adder ADD 2 via the line 5.3.2. and on the other hand the subtracting unit SUB is activated, via the command line 5.3.1, and then accepts the result ΣADD 2, which is present via signal line 5.3, of the adder ADD 2 and, via line 5.2.0, the content QDIV 1_v of the digital memory DSP 2, and forms the difference. In this arrangement, the result ADIV 1_v was obtained during the arithmetic operations triggered by the preceding output pulse Jv 4.1.1 and transferred into the digital memory DSP 2 during the present output pulse J 4.1.1 by activating the former via the pulse line 4.4 whilst the currently present result QDIV 1 is only

transferred into the digital memory DSP 2 with the next following output pulse J_N 4.1.1.

After completion of the arithmetic operation, the subtracting unit SUB activates, via the command line 5.4.1, the multiplier MULT 1, which forms the product from the result DSUB, present via the signal line 5.4, and the result of the multiplier MULT 2, present via the input line 3.4.0. The result of the multiplier MULT 2 is the product of the sampling period T of the sampling clock frequency 3.2.1 - which is present at the multiplier MULT 2 via the line 3.4 - and the number of transmitter divisions 1.1.1 (=number of teeth or markings) - which is input to the multiplier MULT 2 via the input line 5.7; the result is thus a signal-generator-specific product since it takes into consideration the individual-case-dependent construction of the transmitter 1.1 which, for example, could also execute a translatorial movement. Since both the sampling period T, which is set at 3.2., and the number of transmitter divisions 1.1. are known, the product could also be manually formed from these and input as amount to the multiplier MULT 1; the multiplier MULT 2 could then be omitted.

After completion of the arithmetic operation, the multiplier MULT 1 activates, via the command line 5.5.1, the divider DIV 2, which them forms the quotient QDIV 2 from the value "60" present via the input line 5.8 and the PMULT 1 result present via the signal lines 5.8 and the PMULT 1 result present via the signal line 5.5. The input value "60" is produced by the fact that the result PMULT 1 is present in "seconds per revolution" and the result QDIV 2 can be obtained in "revolutions per minute" by means of the subsequent divider DIV 2 and can be displayed on a corresponding component 5.9.

It can be seen that the amplitude values of the signal 1.3 are examined for zero transitions with a falling edge, as a result of which zero point errors are largely compensated during the A/D conversion. Whilst in the illustrative embodiment, therefore, an output pulse J

4.1.1 is always generated, and thus an arithmetic operation run is initiated in the evaluating unit 5, whenever the sinusoidal signal changes from the positive to the negative half wave (falling edge), the amplitude values of the signal 1.3 can be examined for zero transitions with a rising edge - transition from the negative to the positive half wave - when the sign signal supplied to the flip-flop stage 4.1 via the sign line 3.7 is alternatively conducted via the inverter 4.,3 by switching the change-over switch 4.2 over.

CLAIMS:

1. A device for measuring the frequency of a sinusoidal signal generated by a signal generator for measuring the rotational speed of a shaft by means of the signal generated by a signal generator comprising a transmitter which revolves with the shaft and has uniform divisions and a sensor, which device includes a signal processing unit containing an oscillator, A/D converter, counter and memory, the sinusoidal signal being supplied, in operation, to the A/D converter of the signal processing unit, which converter is activated by the oscillator with a constant but adjustable sampling clock frequency - which is higher than the signal frequency - and which in each case forms from the sinusoidal signal digital values which are associated with the sampling clock pulses,wherein

- the A/D converter applies the digital values DW to its outputs in accordance with sign VZ and absolute value AW, the sign VZ being supplied to a flip-flop stage,

- and, triggered by each sampling clock pulse AT of the oscillator via a clock line, on the one hand both a first digital memory (DSP 1) is activated which then accepts the absolute value AW of the digital value formed during the preceding clock pulse which happens to be present at the output of the A/D converter, and supplies this value both to an adder (ADD 1) and to a divider (DIV 1), and the counter (Z) is incremented by "1", the incremented count being supplied to an adder (ADD 2), on the other hand the A/D converter is activated, and now forms the next digital value and applies the latter to its outputs in accordance with sign VZ and absolute value AW, this next absolute value AW also being supplied to the adder (ADD 1),

- and an output pulse is only generated by the flip-flop stage when the sign VZ changes from positive to negative or vice-versa, which output pulse activates both the adder (ADD 1) and a second digital memory (DSP 2) via a pulse line, whereupon the adder (ADD 1) adds the

absolute value (AW +) of the last positive digital value, supplied by the digital memory (DSP 1), to the absolute value (AW -) of the first negative digital value and, after completion of the arithmetic operation, activates the divider (DIV 1), which forms the quotient of the absolute value (AW +) of the last positive digital value and the result $\leq$ ADD 1 of the adder (ADD 1), and, after completion of the arithmetic operation, activates the adder (ADD 2), which adds the result Q DIV 1 of the divider (DIV 1) to the count Zn reached between the preceding (J_v) and the present output pulse (J), when the first negative digital value is present, and, after completion of the arithmetic operation, on the one hand resets the counter (Z) to "0" and on the other hand activates a subtracting unit (SUB) which forms the difference of the result $\leq$ ADD 2 of the adder (ADD 2) and the content Q DIV1$_v$ of the digital memory (DSP 2),
the result Q DIV 1$_v$ having been obtained in the arithmetic operations triggered by the preceding output pulse (J_v) and transferred into the digital memory (DSP 2) during the present output pulse (J), whilst the present result QDIV 1 is only transferred into the digital memory (DSP 2) during the subsequent output pulse (J_N),
and, after completion of the arithmetic operation, activates a multiplier (MULT 1) which forms the product of the result SDSUB of the subtracting unit (SUB) and a signal-generator-specific product present via the input,

- and the frequency or rotational speed is measured again by the output pulse (J_N) generated during the next zero transition of the sinusoidal signal from positive to negative or vice-versa.

2. A device according to claim 1, wherein the scanning clock frequency is a multiple of the signal frequency of the sinusoidal signal.

3. A device according to claim 2, wherein at high rotational speed and in consequence high signal frequency,

a high sampling clock frequency is set.

4. A device according to claim 1, wherein the digital values of the A/D converter are output in binary complement code.

5. A device according to claim 1, wherein the flip-flop stage comprises an edge-controlled, monostable flip-flop.

6. A device according to claim 5, wherein an inverter is connected in series with the flip-flop stage via a change-over switch.

7. A device according to claim 1, wherein an amplifying and/or offset section is connected between the sensor and the A/D converter.

8. A device according to claim 1 or claim 2, wherein a low-pass filter is connected between the sensor and the A/D converter.

9. A device according to claim 1, wherein the signal-generator-specific product is manually input as an amount to the multiplier (MULT 1) via the input.

10. A device according to claim 1, wherein the signal-generator-specific product is supplied to the multiplier (MULT 1) from a multiplier (MULT 2) at the inputs of which the sampling period T of the sampling clock frequency is present via a line and the number of the transmitter divisions via an input line.

11. A device according to claim 10, wherein the multiplier (MULT 1), after completion of its arithmetic operation, activates a divider (DIV 2) which forms the quotient Q DIV 2 (revolution per minute) from the number "60" and the result PMULT 1 (seconds per revolution).

12. A device for measuring the frequency of a sinusoidal signal generated by a signal generator for measuring the rotational speed of a shaft, substantially as described herein, with reference to and as illustrated in, the accompanying drawings.

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